Low-Cost Microprocessor System Hardware Monitor

Analog Devices Confidential **ADM9240**

FEATURES

6 Direct Voltage Measurement Inputs (Including 2 Processor Core Voltages) with On-Chip Attenuators

5 Digital Inputs for VID Bits

LDCM Support

2 Fan Speed Monitoring Inputs

I²C Compatible System Management Bus

Chassis Intrusion Detect

Programmable Reset I/O Pin

Shutdown Mode to Minimize Power Consumption

On-Chip Temperature Sensor

Limit Comparison of all Monitored Values

APPLICATIONS

Network Servers and Personal Computers

Microprocessor-Based Office Equipment

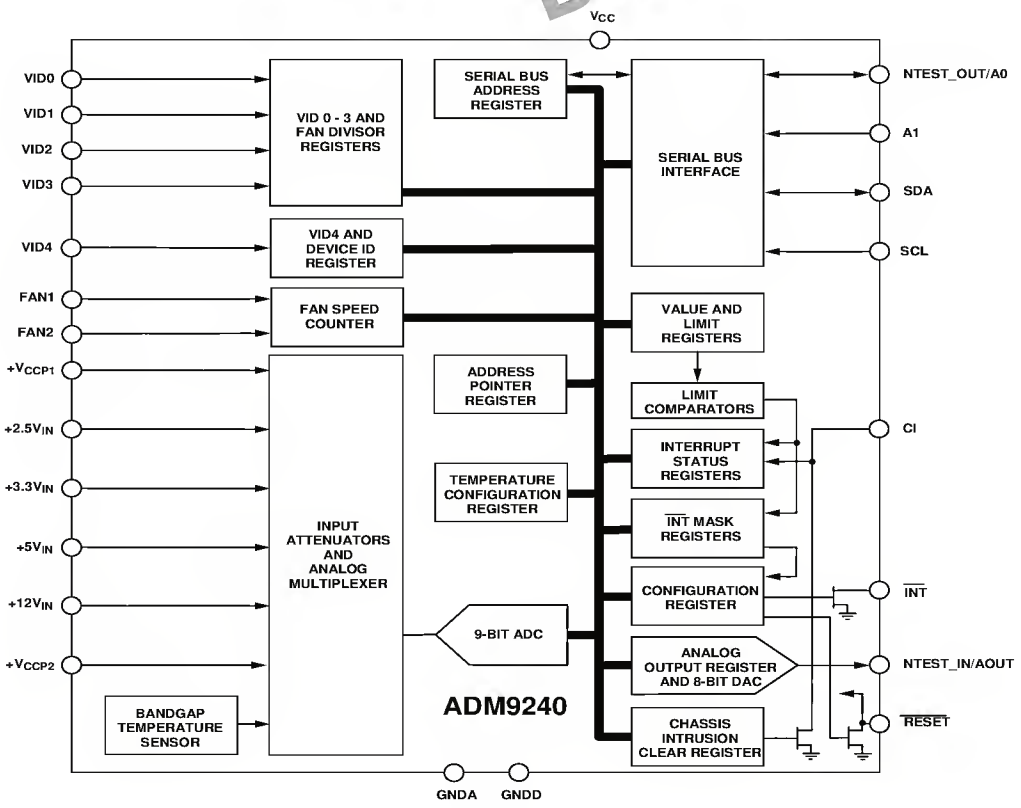
Test Equipment and Measuring Instruments

PRODUCT DESCRIPTION

The ADM9240 is a complete system hardware monitor for microprocessor-based systems, providing measurement and limit comparison of up to four power supplies and two processor core voltages, plus temperature, fan speed and chassis intrusion. Measured values can be read out via an I²C-compatible serial System Management Bus, and values for limit comparisons can be programmed in over the same serial bus. The high-speed successive-approximation ADC allows frequent sampling of all analog channels to ensure a fast interrupt response to any out-of-limit measurement.

The ADM9240's 2.85V to 5.75V supply voltage range, low supply current, and I²C compatible interface make it ideal for a wide range of applications. These include hardware monitoring and protection applications in personal computers, electronic test equipment, and office electronics.

FUNCTIONAL BLOCK DIAGRAM



REVI 11/97

I²C is a registered trademark of Philips Corporation

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 World Wide Web Site: http://www.analog.com
Fax: 617/326-8703

ADM9240–SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage, V_{CC}	2.85	5	5.75	V	
Supply Current, I_{CC}		1.2	2.0	mA	Interface Inactive, ADC Active
		0.5		mA	ADC Inactive, DAC Active
		10		µA	Shutdown Mode
TEMP. -TO-DIGITAL CONVERTER					
Accuracy			±3	°C	-40 °C ≤ T_A ≤ +125°C
			±2	°C	-25 °C ≤ T_A ≤ +100°C
Resolution		±0.5		°C	
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATENUATORS)					
Total Unadjusted Error, TUE			±2	%	Note 3
Differential Non-Linearity, DNL			±1	LSB	
Power Supply Sensitivity		±1		%/V	
Total Monitoring Cycle Time,		311	331	µs	+25°C ≤ T_A ≤ +75°C (Note 4)
		311	353	µs	-10°C ≤ T_A ≤ +100°C (Note 4)
Input Resistance		140		kΩ	Except V_{CCP2}
ANALOG OUTPUT					
Output Voltage Range	0		1.25	V	
Full-Scale Error		±1	±2	%	
Zero Error		2		LSB	No Load
Differential Non-Linearity, DNL			±1	LSB	
Integral Non-Linearity		±1		LSB	
Output Source Current		2		mA	
Output Sink Current		1		mA	
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy			±6	%	+25°C ≤ T_A ≤ +75°C
			±12	%	-10°C ≤ T_A ≤ +100°C
Full-Scale Count			255		
FAN1 and FAN2 Nominal Input RPM		8800		RPM	Divisor = 1, Fan Count = 153 (Note 5)
		4400		RPM	Divisor = 2, Fan Count = 153 (Note 5)
		2200		RPM	Divisor = 3, Fan Count = 153 (Note 5)
		1100		RPM	Divisor = 4, Fan Count = 153 (Note 5)
Internal Clock Frequency	21.1	22.5	23.9	kHz	+25°C ≤ T_A ≤ +75°C
	19.8	22.5	25.2	kHz	-10°C ≤ T_A ≤ +100°C
DIGITAL OUTPUT NTEST_OUT					
Output High Voltage, V_{OH}	2.4			V	I_{OUT} = 5.0mA, V_{CC} = 4.25V - 5.75V
	2.4			V	I_{OUT} = 3.0mA, V_{CC} = 2.85V - 3.45V
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = -5.0mA, V_{CC} = 4.25V - 5.75V
			0.4	V	I_{OUT} = -3.0mA, V_{CC} = 2.85V - 3.45V
OPEN-DRAIN DIGITAL OUTPUTS (INT, RESET, CI)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = -5.0mA, V_{CC} = 5.75V
			0.4	V	I_{OUT} = -3.0mA, V_{CC} = 3.45V
High Level Output Current, I_{OH}		0.1	100	µA	V_{OUT} = V_{CC}
RESET And CI Pulse Width	20	45		ms	

Specifications (Continued)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = -3.0mA, V_{CC} = 4.25V -5.75V
			0.4	V	I_{OUT} = -3.0mA, V_{CC} = 2.85V - 3.45V
High Level Output Current, I_{OH}		0.1	100	µA	V_{OUT} = V_{CC}
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}	0.7 x V_{CC}			V	
Input Low Voltage, V_{IL}			0.3 x V_{CC}	V	
Hysteresis		TBD			
DIGITAL INPUT LOGIC LEVELS (A0, A1, CI, $\overline{\text{RESET}}$,VID0 - VID4, FAN1, FAN2)					
Input High Voltage, V_{IH}	2.4			V	V_{CC} = 4.25V -5.75V
Input Low Voltage, V_{IL}			0.8	V	V_{CC} = 4.25V -5.75V
Input High Voltage, V_{IH}	2.0			V	V_{CC} = 2.85V - 3.45V
Input Low Voltage, V_{IL}			0.4	V	V_{CC} = 2.85V - 3.45V
NTEST_IN					
Input High Voltage, V_{IH}	2.4			V	V_{CC} = 4.25V -5.75V
Input High Voltage, V_{IH}	2.0			V	V_{CC} = 2.85V - 3.45V
DIGITAL INPUTCURRENT(EXCEPT A0, A1)					Note 6
Input High Current, I_{IH}	-1			µA	V_{IN} = V_{CC}
Input Low Current, I_{IL}			1	µA	V_{IN} = 0
Input Capacitance, C_{IN}		20		pF	
SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}			400	kHz	See Figure 1
Glitch Immunity, t_{SW}			50	ns	See Figure 1
Bus Free Time, t_{BUF}	1.3			µs	See Figure 1
Start Setup Time, $t_{SU;STA}$	600			ns	See Figure 1
Start Hold Time, $t_{HD;STA}$	600			ns	See Figure 1
SCL Low Time, t_{LOW}	1.3			µs	See Figure 1
SCL High Time, t_{HIGH}	0.6			µs	See Figure 1
SCL, SDA Rise Time, t_r			300	ns	See Figure 1
SCL, SDA Fall Time, t_f			300	µs	See Figure 1
Data Setup Time, $t_{SU;DAT}$	100			ns	See Figure 1
Data Hold Time, $t_{HD;DAT}$			900	ns	See Figure 1
Data Valid Time, $t_{VD;DAT}$			?	µs	See Figure 1
Stop Setup Time, $t_{SU;STO}$	600			ns	See Figure 1

Specifications subject to change without notice.

NOTES

[1] All voltages are measured with respect to GND, unless otherwise specified

[2] Typicals are at T_J=T_A=25°C and represent most likely parametric norm.

[3] TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC, multiplexer and on-chip input attenuators, including an external series input protection resistor value between zero and 1kΩ.

[4] Total monitoring cycle time is the time taken to measure all six analog inputs plus the temperature sensor. In Normal Mode each channel is measured once, in Average Mode each channel is measured 16 times and the result averaged.

[5] The total fan count is based on 2 pulses per revolution of the fan tachometer output.

[6] A0 and A1 have internal 100kΩ pulldown.

[7] Timing specifications are tested at logic levels of V_{IL} = 0.3 x V_{CC} for a falling edge and V_{IH} = 0.7 x V_{CC} for a rising edge.

ABSOLUTE MAXIMUM RATINGS*

Positive Supply Voltage (V_{CC}) ..... 6.5 V
Voltage on Any Input or Output Pin ....-0.3V to (V_{CC}+0.3V)
(Except analog inputs)
Ground Difference (GND-GNDA) ..... ± 300 mV
Input Current at any pin (Note 2) ..... ±5mA
Package Input Current (Note 2) ..... ±20mA
Maximum Junction Temperature ($T_J$max) ..... 150 °C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature, Soldering
Vapor Phase 60 sec .....+215°C
Infra-Red 15 sec .....+200°C
ESD Rating (Human Body Model) ..... 2000 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

24-Pin Small Outline Package:
θ_{JA} = 50°C/Watt, θ_{JC} = 10°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM9240ARU	-40°C to +125°C	24-Pin TSSOP Package	RU-24

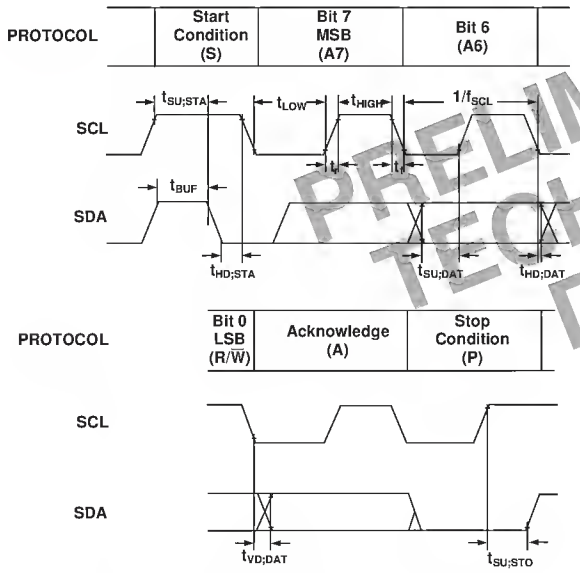
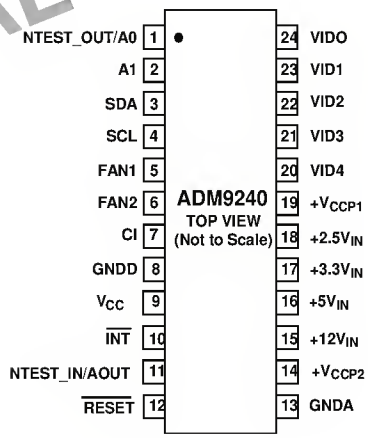


Figure 1. Diagram for Serial Bus Timing

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

PIN NO.	MNEMONIC	DESCRIPTION
1	NTEST_OUT/A0	Digital I/O. The lowest order programmable bit of the Serial Bus Address. This pin functions as an output when doing a NAND Tree test.
2	A1	Digital Input. The highest order programmable bit of the Serial Bus Address.
3	SDA	Digital I/O. Serial Bus bidirectional Data. Open-drain output.
4	SCL	Digital Input. Serial Bus Clock.
5	FAN1	Digital Input. 0 to V_{CC} amplitude fan tachometer input.
6	FAN2	Digital Input. 0 to V_{CC} amplitude fan tachometer input.
7	CI	Digital I/O. An active high input from an external circuit which latches a Chassis Intrusion event. This line can go high without any clamping action regardless of the powered state of the ADM9240. The ADM9240 provides an internal open drain on this line, controlled by Bit 5 of Configuration Register, to provide a minimum 20ms pulse on this line, to reset the external Chassis Intrusion Latch.
8	GNDD	Digital Ground. Internally connected to all of the digital circuitry.
9	V_{CC} (+2.85to+5.75V)	POWER. Typically powered from +3.3V or +5V power rail. Bypass with the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors.
10	INT	Digital Output. Interrupt Request (open drain). The output is enabled when Bit 1 of the Configuration Register is set to 1. The default state is disabled.
11	NTEST_IN/AOUT	Test Input/Analog Output. An active-high input that enables NAND Tree board-level connectivity testing. Refer to section on NAND Tree testing. Used as a analog output when NAND Tree is not selected
12	RESET	Digital I/O. Master Reset, 5 mA driver (open drain), active low output with a 20 ms minimum pulse width. Available when enabled via Bit 4 in Configuration Register. Also acts as reset input when pulled low (e.g. power-on reset).
13	GNDA	Analog Ground. Internally connected to all analog circuitry. The ground reference for all analog inputs.
14	$+V_{CCP2}$	Analog Input. Monitors processor core voltage $+V_{CCP}$ (1.2V - 3.6V).
15	$+12V_{IN}$	Analog Input. Monitors +12 V supply.
16	$+5V_{IN}$	Analog Input. Monitors +5 V supply.
17	$+3.3V_{IN}$	Analog Input. Monitors +3.3 V supply.
18	$+2.5V_{IN}$	Analog Input. Monitors +2.5 V supply.
19	$+V_{CCP1}$	Analog Input. Monitors processor core voltage $+V_{CCP}$ (1.2V - 3.6V).
20	VID4	Digital Input. Voltage supply readouts from the processor. This value is read into the VID4 Status Register.
21	VID3	Digital Input. Voltage supply readouts from the processor. This value is read into the VID0-VID3 Status Register.
22	VID2	Digital Input. Voltage supply readouts from the processor. This value is read into the VID0-VID3 Status Register.
23	VID1	Digital Input. Voltage supply readouts from the processor. This value is read into the VID0-VID3 Status Register.
24	VID0	Digital Input. Voltage supply readouts from the processor. This value is read into the VID0-VID3 Status Register.

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

The ADM9240 is a complete system hardware monitor for microprocessor-based systems. The device communicates with the system via a serial System Management Bus. The serial bus controller has two hardwired address lines for device selection (pins 1 and 2), a serial data line for reading and writing addresses and data (pin 3), and an input line for the serial clock (pin 4). All control and programming functions of the AD9240 are performed over the serial bus.

An on-chip analog-to-digital converter with 6, multiplexed analog inputs measures power supply voltages (+12V, +5V, +3.3V, +2.5V - pins 15 to 18) and processor core voltages $+V_{CCP1}$ and $+V_{CCP2}$ pins 19 and 14). The ADC also accepts input from an on-chip bandgap temperature sensor that monitors system ambient temperature.

Two count inputs are provided for monitoring the speed of fans with tachometer outputs (pins 5 and 6).To accommodate fans with different speeds and different tacho outputs, a divisor of 1, 2 , 4 or 8 can be programmed into the counter.

Five digital inputs (VID4 to VID0 - pins 20 to 24) read the processor Voltage ID code, whilst a chassis intrusion input (pin 7) is provided to detect unauthorised tampering with the equipment.

When the ADM9240 monitoring sequence is started, it cycles sequentially through the measurement of analog inputs and the temperature sensor, while at the same time the fan speed inputs are monitored. Measured values from these inputs are stored in Value Registers. These can be read out over the serial bus, or can be compared with programmed limits stored in the Limit Registers. The results of out of limit comparisons are stored in the Interrupt Status Registers, and will generate an interrupt on the INT line (pin 10).

Any or all of the Interrupt Status Bits can be masked by appropriate programming of the Interrupt Mask Register.

A RESET input/output (pin 12) is provided. Pulling this pin low will reset all ADM9240 internal registers to default values. The ADM9240 can also be programmed to give a low-going 20ms reset pulse at this pin.

The ADM9240 contains an on-chip, 8-bit digital-to-analog converter with an output range of zero to 1.25V (pin 11). This is typically used to implement a temperature-controlled fan by controlling the speed of a fan dependent upon the temperature measured by the on-chip temperature sensor.

Testing of board level connectivity is simplified by providing a NAND tree test function. The analog output (pin 11) also doubles as a NAND test input, while pin 1 doubles as a NAND tree output.

INTERNAL REGISTERS OF THE ADM9240

A brief description of the ADM9240's principal internal registers is given below. More detailed information on the function of each register is given in Tables 5 to 17, starting on page 19.

Serial Address Register: The serial Address Register stores the serial bus address of the ADM9240.

Address Pointer Register: This register contains the address that selects one of the other internal registers. When writing to the ADM9240, the first byte of data is always a register address, which is written to the Address Pointer Register.

Configuration Register: Provides control and configuration.

Interrupt (INT) Status Registers: Two registers to provide status of each limit or Interrupt event.

Interrupt (INT) Mask Registers: Allow masking of individual Interrupt sources, as well as separate masking for each of the hardware Interrupt outputs.

Temperature Configuration Register: The configuration of the temperature interrupt is controlled by the lower 3 bits of this register. Bit 7 contains the lowest bit of the temperature reading.

VID Registers: The status of the VID0 to VID4 pins of the processor can be written to and read from these registers. The ADM9240 does not process or make use of this data in any way, but it may be used by another processor in multi-processor systems. Divisor values for fan-speed measurement are also stored in one of these registers.

Value and Limit Registers: The results of analog input, temperature and fan speed measurements are stored in these registers, along with their limit values.

Analog Output Register: The code controlling the analog output DAC is stored in this register.

Chassis Intrusion Clear Register: The A signal latched on the Chassis Intrusion pin can be cleared by writing a 1 to bit 7 of this register.

SERIAL BUS INTERFACE

Control of the ADM9240 is carried out via the serial bus. The ADM9240 is connected to this bus as a slave device, under the control of a master device, e.g. the processor.

Like all devices using this protocol, the ADM9240 has a 7-bit serial bus address. When the device is powered up, it will do so with a default serial bus address. The five MSB's of the address are set to 01011, the two LSB's are determined by the logical states of pin 1(NTESTOUT/ A0) and pin 2 (A1) at power up. These pins have internal 100kΩ pulldown resistors, so if they are left open-circuit the default address will be 0101100.

The facility to make hardwired changes to A1 and A0 allows the user to avoid conflicts with other devices sharing the same serial bus, for example if more than one ADM9240 is used in a system. Once the ADM9240 has been powered up, the 5 MSB's of the serial bus address may be changed by writing a 7-bit word to the serial Address Pointer Register (the hardwired values of A0 and A1 cannot be overwritten). Thereafter, the new serial bus address must be used to select the ADM9240, until it is changed again, or the device is powered off.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA whilst the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit address (MSB first) plus a R/W bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle whilst the selected device waits for data to be read from or written to it. if the R/W bit is a 0 then the master will write to the slave device. If the R/W bit is a 1 the master will read from the slave device.

2. Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge Bit from the slave device.Transitions on the data line must

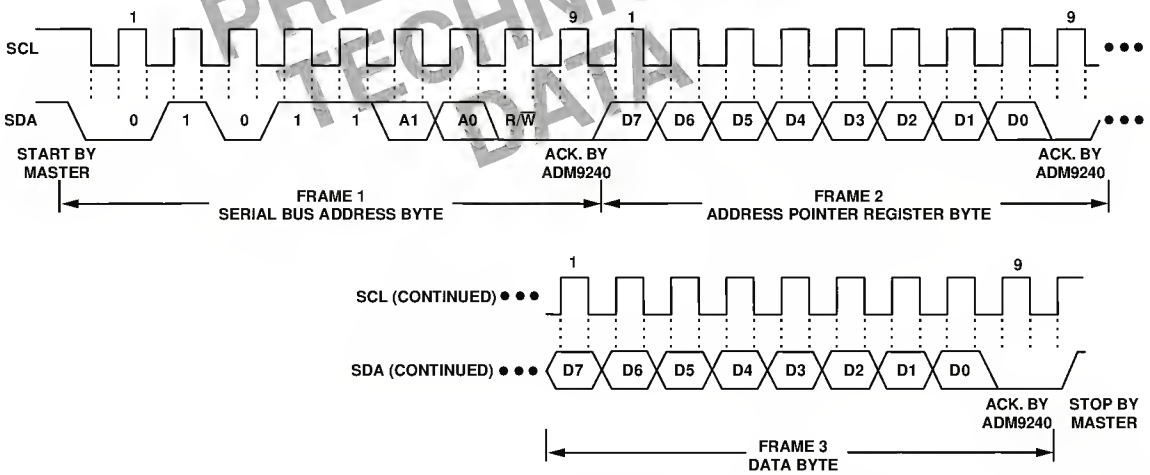


Figure 2a. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

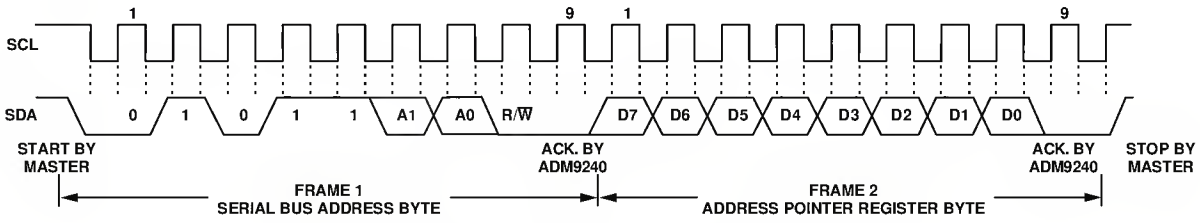


Figure 2b. Writing to the Address Pointer Register only

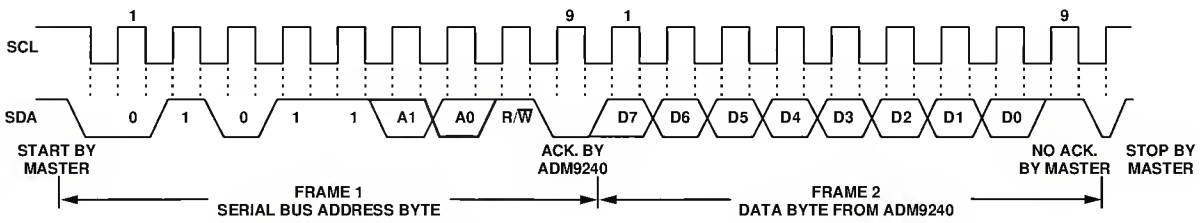


Figure 2c. Reading Data from a Previously Selected Register

occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowldge bit by pulling the data line high during the low period before the 9th clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the case of the ADM9240, write operations contain either one or two bytes, and read operations contain one byte, and perform the following functions:

To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, then the write operation contains a second data byte that is written to the register selected by the address pointer register.

This is illustrated in figure 2a. The device address is sent over the bus followed by R/W set to 0. This is followed by two data bytes.The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. the second data byte is the data to be written to the internal data register.

When reading data from a register there are two possibilities:

1. If the ADM9240's Address Pointer Register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADM9240 as before, but only the data byte containing the register address is sent, as data is not to be written to the register. This is shown in figure 2b.

   A read operation is then performed consisting of the serial bus address, R/W bit set to 1, followed by the data byte read from the data register. This is shown in figure 2c.

2. If the Address Pointer Register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the Address Pointer Register, so figure 2b can be omitted.

Notes:

1. Although it is possible to read a data byte from a data register without first writing to the Address Pointer Register, if the Address Pointer Register is already at the correct value, it is not possible to write data to a register without writing to the Address Pointer Register, because the first data byte of a write is always written to the Address Pointer Register.
2. In figures 2a to 2c, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are hardwired to either logic 0 or logic 1.

ANALOG INPUTS

The ADM9240 has six analog inputs. Four of these are dedicated to monitoring the following power supply voltages:

+12V, +5V, +3.3V, +2.5V.

These inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of 10 bits, but only 8 bits are used for the voltage measurement and limit comparison. The basic input range of the ADC is zero to 2.5V, and the power supply inputs are scaled by on-chip attenuators such that such that the ADC produces an output of 3/4 x full-scale scale or 192 decimal, when the input voltage is at its nominal value. The use of on-chip scaling guarantees accuracy and removes the need for precision external resistors.

The input ranges of the analog inputs are shown in more detail in Table 1, overleaf

The $+V_{CCP1}$ and $+V_{CCP2}$ inputs are used to measure processor core voltages, which vary from 1.2V-3.6V. Since voltages below 1.2V are not of interest, the measurement range is scaled and offset so that 1 LSB corresponds to 9.4mV, a conversion result of 00000000 corresponds to 1.2V, and a conversion result of 11111111 (255 decimal) corresponds to 3.6V.

TABLE 1. A/D OUTPUT CODE VS. V_{IN}

Input Voltage						A/D Output	
$+12V_{IN}$	$+5V_{IN}$	$+3.3V_{IN}$	$+2.5V_{IN}$	$+V_{CCP1}$	$+V_{CCP2}$	Decimal	Binary
<0.062	<0.026	<0.0172	<0.013	<1.209	<1.209	0	00000000
0.062 - 0.125	0.026 - 0.052	0.017 - 0.034	0.013 - 0.026	1.209 - 1.218	1.209 - 1.218	1	00000001
0.125 - 0.187	0.052 - 0.078	0.034 - 0.052	0.026 - 0.039	1.218 - 1.228	1.218 - 1.228	2	00000010
0.188 - 0.250	0.078 - 0.104	0.052 - 0.069	0.039 - 0.052	1.228 - 1.237	1.228 - 1.237	3	00000011
0.250 - 0.313	0.104 - 0.130	0.069 - 0.086	0.052 - 0.065	1.237 - 1.247	1.237 - 1.247	4	00000100
0.313 - 0.375	0.130 - 0.156	0.086 - 0.103	0.065 - 0.078	1.247 - 1.256	1.247 - 1.256	5	00000101
0.375 - 0.438	0.156 - 0.182	0.103 - 0.120	0.078 - 0.091	1.256 - 1.265	1.256 - 1.265	6	00000110
0.438 - 0.500	0.182 - 0.208	0.120 - 0.138	0.091 - 0.104	1.265 - 1.275	1.265 - 1.275	7	00000111
0.500 - 0563	0.208 - 0.234	0.138 - 0.155	0.104 - 0.117	1.275 - 1.285	1.275 - 1.285	8	00001000
			•				
			•				
			•				
4.000 - 4.063	1.666 - 1.692	1.100 - 1.117	0.833 - 0.846	1.800 - 1.809	1.800 - 1.809	64 (1/4-scale)	01000000
			•				
			•				
			•				
8.000 - 8.063	3.330 - 3.560	2.200 - 2.217	1.667 - 1.680	2.400 - 2.4095	2.400 - 2.409	128 (1/2-scale)	10000000
			•				
			•				
			•				
12.000 - 12.063	5.000 - 5.026	3.300 - 3.317	2.500 - 2.513	3.00 - 3.009	3.00 - 3.009	192 (3/4 scale)	11000000
			•				
			•				
			•				
15.312 - 15.375	6.380 - 6.406	4.210 - 4.230	3.190 - 3.203	3.495 - 3.505	3.495 - 3.505	245	11110101
15.375 - 15.437	6.406 - 6.432	4.230 - 4.245	3.203 - 3.216	3.505 - 3.515	3.505 - 3.515	246	11110110
15.437 - 15.500	6.432 - 6.458	4.245 - 4.263	3.216 - 3.229	3.515 - 3.524	3.515 - 3.524	247	11110111
15.500 - 15.563	6.458 - 6.484	4.263 - 4.280	3.229 - 3.242	3.524 - 3.534	3.524 - 3.534	248	11111000
15.562 - 15.625	6.484 - 6.510	4.280 - 4.300	3.242 - 3.2551	3.534 - 3.543	3.534 - 3.543	249	11111001
15.625 - 15.688	5.510 - 6.536	4.300 - 4.314	3.255 - 3.268	3.543 - 3.552	3.543 - 3.552	250	11111010
15.688 - 15.750	6.536 - 6.562	4.314 - 4.33	3.268 - 3.281	3.552 - 3.561	3.552 - 3.561	251	11111011
15.750 - 15.812	6.562 - 6.588	4.331 - 4.348	3.281 - 3.294	3.561 - 3.571	3.561 - 3.571	252	11111100
15.812 - 15.875	6.588 - 6.615	4.348 - 4.366	3.294 - 3.397	3.571 - 3.581	3.571 - 3.581	253	11111101
15.875 - 15.938	6.615 - 6.640	4.366 - 4.383	3.307 - 3.320	3.581 - 3.590	3.581 - 3.590	254	11111110
>15.938	>6.640	>4.383	>3.320	>3.590	>3.590	255	11111111

INPUT CIRCUITS

The input circuits for the analog inputs are shown in figure 3. Each input circuit consists of an input protection diode (except for the +12V input), an attenuator, plus a capacitor to form a first-order lowpass filter which gives the input some immunity to noise.

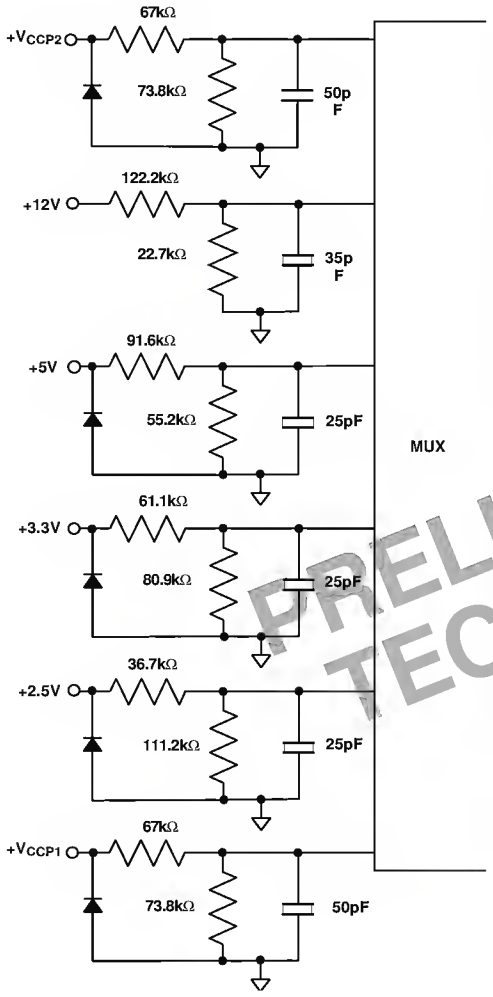


Figure 3. Structure of Analog Inputs

SETTING OTHER INPUT RANGES

If any of the inputs is unused, and there is a requirement for monitoring another power supply such as -12V, then the input range of the unused input can easily be scaled and offset to accommodate this. For example, if only one processor core voltage is to be monitored, then the unused V_{CCP} input can be used to monitor another supply voltage, for example -12V.

To monitor a negative voltage such as -12V the input voltage must first be converted to a positive voltage. The simplest way to do this is simply to attenuate and offset the voltage, as shown in figure 4.

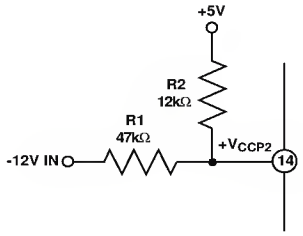


Figure 4. Scaling V_{CCP2} to -12V

This is a simple and cheap solution, but the following points should be noted.

1. Since the input signal is not inverted, an increase in the magnitude of the -12V supply (going more negative, will cause the input voltage to fall and give a lower output code from the ADC. Conversely, a decrease in the magnitude of the -12V supply will cause the ADC code to increase. This means that the upper and lower limits will be transposed.
2. Since the offset voltage is derived from the +5V supply, variations in this supply will affect the ADC code. It is therefore a good idea to read the value of the +5V supply and adjust the limits for the -12V supply accordingly.
3. The on-chip input attenuators will load the external attenuator. This can be compensated for in the calculations, but the values of the on-chip attenuator resistors are not precise and they have fairly large temperature coefficients. The values of the external resistors should therefore be small compared to the on-chip input resistance of nominally 140kΩ.
4. This technique can be applied to any other unused input.
5. In figure 3 the resistor values are chosen so that the nominal supply voltage of -12V corresponds to approximately half-scale on the ADC. With the reistor values shown, the input voltage range is approximately -2.35 to -14.95V

   Any variation in the +5V supply is attenuated by the inverse ratio of the attenuator (x 0.81), so the high limit for the -12V supply should be increased by 0.81V for every 1V increase in the 5V supply and decreased by 0.81V for every 1V decrease in the +5V supply. The low limit should be changed in the opposite sense

TEMPERATURE MEASUREMENT SYSTEM

The ADM9240 contains an on-chip bandgap temperature sensor. The on-chip ADC performs 9-bit conversions on the output of this sensor and outputs the temperature data in 9-bit two's complement format, but only the 8 most significant bits are used for temperature limit comparison. The full 9-bit temperature data can be obtained by reading the 8 MSB's from the Temperature Value Register (address 27h) and the LSB from bit 7 of the Temperature Configuration Register (address 4Bh).

The format of the temperature data is shown in Table 2, opposite. Theoretically, the temperature sensor and ADC can measure temperatures from -128°C to +127°C with a resolution of 0.5°C, although temperatures below -40°C and above +125°C are outside the operating temperature range of the device.

LIMIT VALUES

Limit values for analog measurements can be stored in the appropriate limit registers. In the case of voltage measurements, high and low limits can be stored so that an interrupt request will be generated if the measured value goes above or below acceptable values. In the case of temperature A Hot Temperature Limit can be programmed, and a Hot Temperature Hysteresis Limit, which will usually be some degrees lower. This can be useful as it allows the system to be shut down when the hot limit is exceeded, and re-started automatically when it has cooled down to a safe temperature.

TABLE 2. TEMPERATURE DATA FORMAT

Temperature	Digital Output
-128 °C	1 0000 0000
-125 °C	1 0000 0110
-100 °C	1 0011 1000
-75 °C	1 0110 1010
-50 °C	1 1001 1100
-25 °C	1 1100 1110
-0.5 °C	1 1111 1111
0 °C	0 0000 0000
+0.5 °C	0 0000 0001
+10 °C	0 0001 0100
+25 °C	0 0011 0010
+50 °C	0 0110 0100
+75 °C	0 1001 0110
+100 °C	0 1100 1000
+125 °C	0 1111 1010
+127 °C	0 1111 1111

MONITORING CYCLE TIME

The monitoring cycle begins when a one is written to the Start Bit (bit 0), and a zero to the INT_Clear Bit (bit 3) of the Configuration Register. INT_Enable (Bit 1) should be set to one to enable the INT output. The ADC measures each analog input in turn, starting with V_{CCP2} and finishing with the on-chip temperature sensor. As each measurementis completed the result is automatically stored in the appropriate value register. This "round-robin" monitoring cycle continues until it is disabled by writing a 0 to bit 0 of the Configuration Register.

The counter controlling the multiplexer is driven by an on-chip clock of nominally 22.5kHz, so the entire measurement sequence takes (nominally):

44.4µs x 7 = 310.8µs.

This rapid sampling of the analog inputs ensures a quick response in the event of any input going out of limits, unlike other monitoring chips that employ slower ADCs.

When a monitoring cycle is started, monitoring of the fan speed inputs begins at the same time as monitoring of the analog inputs. However, the two monitoring cycles are not synchronised in any way, and the monitoring cycle time for the fan inputs is dependent on fan speed and much slower than for the analog inputs. For more details see the section on "FAN SPEED MEASUREMENT".

AVERAGING MODE

Instead of taking a single measurement on each analog channel, the ADM9240 may be configured to take 16 measurements on each channel and average the result. This reduces the possibility of an out of limit interrupt being triggered by a single noise spike, but it does, of course, increase the monitoring time to 5ms.

The averaging mode is selected by setting bit 7 of the Test Mode Register to 1.

INPUT SAFETY

Scaling of the analog inputs is performed on chip, so external attenuators are normally not required. However, since the power supply voltages will appear directly at the pins, its is advisable to add small small external resistors in series with the supply traces to the chip to prevent damaging the traces or power supplies should a accidental short such as a probe connect two power supplies together.

As the resistors will form part of the input attenuators, they will affect the accuracy of the analog measurement if their value is too high. The analog input channels are calibrated assuming an external series resistor of 500Ω, and the accuracy will remain within specification for any value from zero to 1kΩ, so a standard 510Ω resistor is suitable.

The worst such accident would be connecting -12V to +12V - a total of 24V difference, with the series resistors this would draw a maximum current of approx. 24mA.

ANALOG OUTPUT

The ADM9240 has a single analog output from a unsigned 8 bit DAC which produces 0 - 1.25V, this is amplified and buffered with external circuitry such as an op-amp and transistor to provide fan speed control. this register is set to 0xFF during power-on reset, which produces maximum fan speed.

This voltage must be scaled and have a source current capability of at least 250mA which is needed to drive the fans. A suitable circuit is given in Figure 5.

Care must be taken when choosing the op-amp to ensure that its input common-mode range and output voltage swing are suitable.

The op-amp may be powered from the +12V rail alone or from ±12V. If it is powered from +12V then the input common-mode range should include ground to accommodate the minimum output voltage of the DAC, and the output voltage should swing below 0.6V to ensure that the transistor can be turned fully off.

If the op-amp is powered from -12V then precautions such as a clamp diode to ground may be needed to prevent the base-emitter junction of the transistor being reverse-biased in the unlikely event that the output of the op-amp should swing negative for any reason.

The positive output swing of the op-amp should be as close to +12V as possible so that the maximum voltage can be obtained from the transistor. Even if the op-amp swings to the rail, the maximum voltage from the emitter of the transistor will be about 11.4V. typical values for this condition would be:

Gain = 11.4/1.25 = 9.12 = 1 + R1/R2

R1 = 82kΩ, R2 = 10kΩ (nearest preferred value)

giving an actual gain of 9.2.

The transistor should have a reasonably high h_{fe} to avoid its base current pulling down the output of the op-amp, it must have an I_{CMAX} greater than the maximum fan current, and be capable of dissipating power due to the voltage dropped across it when the fan is not operating at full-speed. Depending on the fan parameters, some suitable devices would be 2N2219A, 2N3019, or ZTX450.

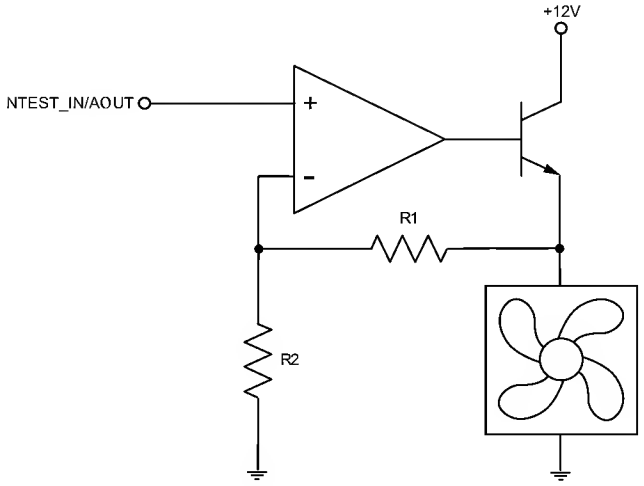


Figure 5. Analog Output Driving Fan

LAYOUT AND GROUNDING

Analog inputs will provide best accuracy when referred to the GNDA pin. A separate, low-impedance ground plane for analog ground, which provides a ground point for the voltage dividers and analog components, will provide best performance but is not mandatory. Analog components such as voltage dividers should be located physically as close as possible to the ADM9240.

The power supply bypass, the parallel combination of 10µF (electrolytic or tantalum) and 0.1µF (ceramic) bypass capacitors connected between pin 9 and ground, should also be located as close as possible to the ADM9240.

FAN INPUTS

Two inputs are provide for monitoring the condition of cooling fans. Signal conditioning in the ADM9240 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to V_{CC}. In the event that these inputs are supplied from fan outputs which exceed 0 to V_{CC}, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figures 6a to 6c show circuits for most common fan tacho outputs.

If the fan tacho output has a resistive pullup to V_{CC} then it can be connected directly to the fan input, as shown in figure 6a.

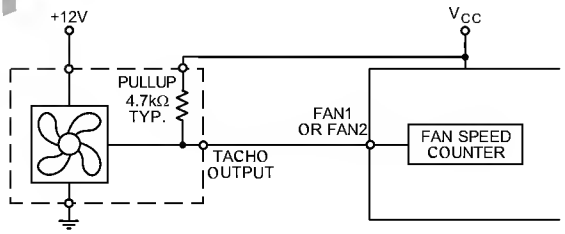


Figure 6a. Fan With Tach Pullup To +V_{CC}.

If the fan output has a resistive pullup to +12V (or other voltage greater than V_{CC}) then the fan output can be clamped with a zener diode, as shown in figure 6b. The zener voltage should be chosen so that it is greater than V_{IH} but less than V_{CC}, allowing for the voltage tolerance of the zener. A value of about 0.8 x V_{CC} is suitable.

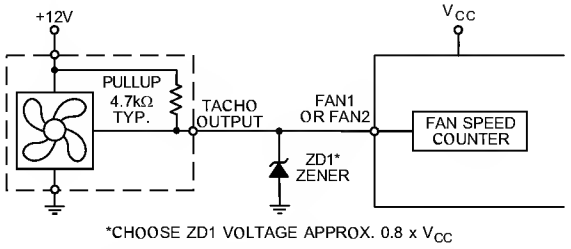


Figure 6b. Fan with Tach. Pullup to Voltage >V_{CC} e.g. 12V) Clamped with Zener Diode

If the fan has a strong pullup (less than 1kΩ) to +12V, or a totem-pole output, then a series resistor can be added to limit the zener current, as shown in figure 6c. Alterna-

tively, a resistive attenuator may be used, as shown in figure 6d.

R1 and R2 should be chosen such that:

$2V < V_{PULLUP} \times R2/(R_{PULLUP} + R1 + R2) < V_{CC}$

If the value of the pullup resistor is not known then the value of R1 and R2 should be made fairly large, but not so large that the input leakage current will cause a large voltage drop across them.

With a pullup voltage of 12V and pullup resistor less than 1kΩ, suitable values for R1 and R2 would be 100kΩ and 47kΩ.This will give a high input voltage of 3.83V.

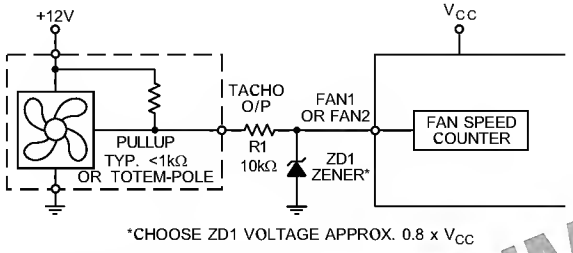


Figure 6c. Fan with Strong Tach. Pullup to >V_{CC} or Totem-Pole Output, Clamped with Zener and Resistor

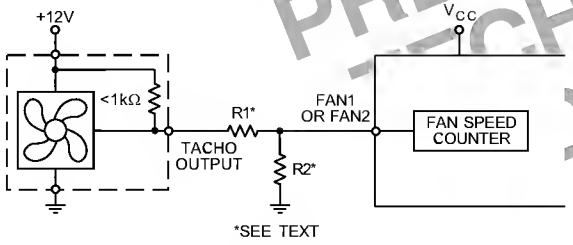


Figure 6d. Fan with Strong Tach. Pullup to >V_{CC} or Totem-Pole Output, Attenuated with R1/R2

INPUT CURRENT LIMITING

If the fans are powered while the ADM9240 is unpowered, then the inputs of the ADM9240 will try to clamp the fan output voltage. In this case the input current must be limited to less than the maximum value in the Absolute Maximum Ratings table. The pullup resistor of the fan tacho output may provide this current limiting, but if its value is too low then it may be necessary to add additional resistance in series with the fan input pins.

FAN SPEED MEASUREMENT

The fan counter does not count the fan tacho output pulses directly, because the fan speed may be less than 1000 RPM and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 22.5kHz oscillator into the input of an 8-bit counter for two periods of the fan tacho output, as shown in figure 7, so the accumulated count is actually proportional to the fan tacho period and inversely proportional to the fan speed.

The monitoring cycle begins when a one is written to the Start Bit (bit 0), and a zero to the INT_Clear Bit (bit 3) of the Configuration Register. INT_Enable (Bit 1) should be set to one to enable the INT output. The measurement begins on the rising edge of a fan tacho pulse, and ends on the next-but-one rising edge. Once the fan speeds have been measured, they will be stored in the Fan Speed Value Registers and can be read at any time. The measurements will be updated as long as the monitoring cycle continues.

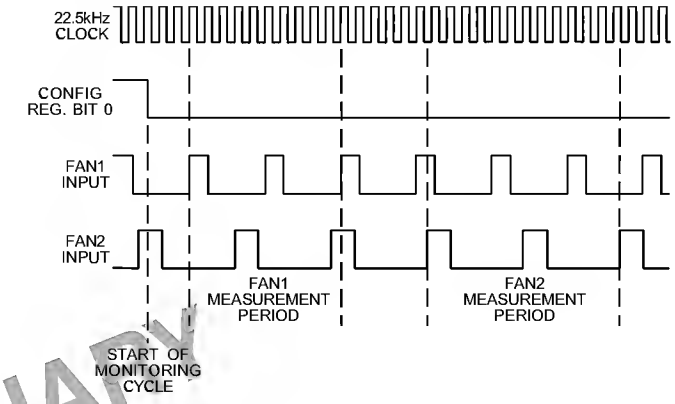


Figure 7. Fan Speed Measurement

To accommodate fans of different speed and/or different numbers of output pulses per revolution, a pre-scaler (divisor) of 1, 2, 4 or 8 may be added before the counter. The default value is 2, which gives a count of 153 for a fan running at 4400 RPM producing two output pulses per revolution.

The count is calculated by the equation:

$Count = 1.35 \times 10^6/(RPM \times Divisor)$

For constant speed fans, fan failure is normally considered to have occurred when the speed drops below 70% of nominal, which would correspond to a count of 219. Full-scale (255) would be reached if the fan speed fell to 60% of its nominal value. For temperature-controlled variable speed fans the situation will be different.

Table 2 shows the relationship between fan speed and time per revolution at 60%, 70% and 100% of nominal RPM for fan speeds of 1100, 2200, 4400 and 8800 RPM, and the divisor that would be used for each of these fans, based on two tacho pulses per revolution.

TABLE 2. FAN SPEEDS AND DIVISORS

Divisor	Nominal RPM	Time per rev (ms)	70% RPM	Time per rev (70%) (ms)	60% RPM	Time per rev (60%) (ms)
÷ 1	8800	6.82	6160	9.74	5280	11.36
÷ 2	4400	13.64	3080	19.48	2640	22.73
÷ 4	2200	27.27	1540	38.96	1320	45.45
÷ 8	1100	54.54	770	77.92	660	90.9

Note that Fan 1 and Fan 2 Divisors are programmed into bits 4 to 7 of the VID 0 - 3/Fan Divisor Register.

LIMIT VALUES

Fans in general will not overspeed if run from the correct voltage, so the failure condition of interest is underspeed due to electrical or mechanical failure. For this reason only low-speed limits are programmed into the limit registers for the fans. It should be noted that, since fan period rather than speed is being measured, a fan failure interrupt will occur when the measurement *exceeds* the limit value.

MONITORING CYCLE TIME

The monitoring cycle time depends on the fan speed and number of tacho output pulses per revolution. Two complete periods of the fan tacho output (three rising edges) are required for each fan measurement. Therefore, if the start of a fan measurement just misses a rising edge, the measurement can taken almost three tacho periods. In order to read a valid result from the fan value registers, the total monitoring time allowed after starting the monitoring cycle should therefore be three tacho periods of FAN1 plus three tacho PERIODS of FAN2 at the lowest normal fan speed.

Although the fan monitoring cycle and the analog input monitoring cycle are started together, they are not synchronised in any other way.

FAN MANUFACTURERS

Manufacturers of cooling fans with tachometer outputs are listed below:

NMB Tech

9730 Independence Ave.

Chatsworth, California 91311

818-341-3355

818-341-8207

Model	Frame Size	Airflow CFM
2408NL	2.36 in sq. X 0.79 in (60mm sq. X 20mm)	9-16
2410ML	2.36 in sq. X 0.98 in (60mm sq. X 25mm)	14-25
3108NL	3.15 in sq. X 0.79 in (80mm sq. X 20mm)	25-42
3110KL	3.15 in sq. X 0.98 in (80mm sq. X 25mm)	25-40

Mechatronis Inc.

P.O. Box 20

Mercer Island, WA 98040

800-453-4569

Models - Various sizes available with tach output option.

Sanyo Denki/Keymarc Electronics

2310 205th, Suite 101

Torrance, CA 90501

310-212-7724

Models - 109P Series

CHASSIS INTRUSION INPUT

The Chassis Intrusion input is an active high input/open-drain output intended for detection and signalling of unauthorised tampering with the system. An external circuit powered from the system's CMOS backup battery is used to detect and latch a chassis intrusion event, whether the system is powered up or not. Once a chassis intrusion has been detected and latched, the CI input will generate an interrupt when the system is powered up

The actual detection of chassis intrusion is performed by an external circuit that will detect (for example), when the cover has been removed. A wide variety of techniques may be used for the detection, for example:

- Microswitch that opens or closes when the cover is re moved.
- Reed switch operated by magnet fixed to the cover
- Hall-effect switch operated by magnet fixed to the cover.
- Phototransistor that detects light when cover is removed.

The chassis intrusion interrupt will remain asserted until the external detection circuit is reset. This can be achieved by setting bit 5 of the Configuration Register, or bit 7 of the Chassis Intrusion Clear Register to one, which will cause the CI pin to be pulled low for at least 20ms. These register bits are self-clearing.

The chassis intrusion circuit should be designed so that it can be reset by pulling its output low. A suitable chassis intrusion circuit using a phototransistor is shown in figure 8. Light falling on the phototransistor when the PC cover is removed will cause it to turn on and pull up the input of N1, thus setting the latch N3/N4. After the cover is replaced, a low reset on the CI output will pull down the input of N4, resetting the latch.

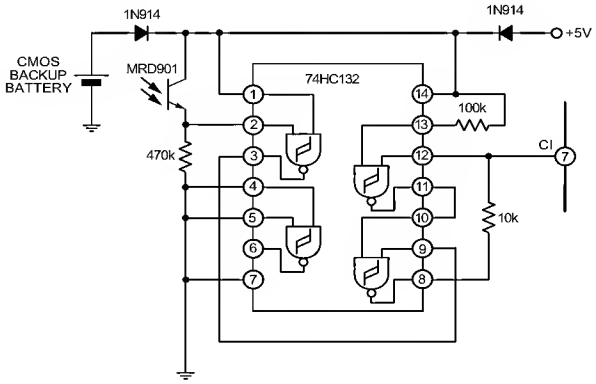


Figure 8a. Chassis Intrusion Detector and Latch

The Chassis Intrusion input can also be used for other types of alarm input. Figure 8b shows a temperature alarm circuit using an AD22105 temperature switch sensor. This produces a low-going output when the preset temperature is exceeded, so the output is inverted by Q1 to make it compatible with the CI input. Q1 can by almost any small-signal NPN transistor, or a TTL or CMOS inverter gate may be used if one is available. See the AD22105 data sheet for information on selecting R_{SET}.

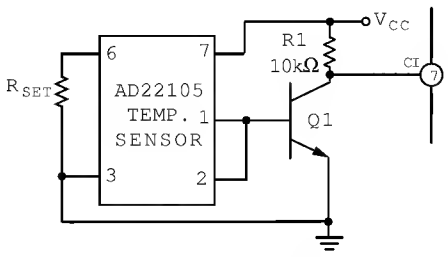


Figure 8b. Using the CI Input with a Temperature Sensor

Note: The chassis intrusion input does not have a protective clamp diode to V_{CC}, as this could pull down the chassis intrusion latch and reset it when the ADM9240 was powered down.

THE ADM9240 INTERRUPT STRUCTURE

The Interrupt Structure of the ADM9240 is shown in Figure 9. As each measurement value is obtained and stored in the appropriate value register, the value and the limits from the corresponding limit registers are fed to the high and low limit comparators. The result of each comparison (1 = out of limit, 0 = in limit) is routed to the corresponding bit input of the Interrupt Status Registers via a data demultiplexer, and used to set that bit high or low as appropriate.

The Interrupt Mask Registers have bits corresponding to each of the Interrupt Status Register Bits. Setting an Interrupt Mask Bit high forces the corresponding Status Bit output low, whilst setting an Interrupt Mask Bit low allows the corresponding Status Bit to be asserted. After masking, the status bits are all OR'd together to produce the INT output, which will pull low if any unmasked status bit goes high, i.e. when any measured value goes out of limit.

The INT output is enabled when Bit 1 of the Confugration Register (INT Enable) is high, and Bit 3 (INT_Clear) is low.

INTERRUPT CLEARING

Reading an Interrupt Status Register will output the contents of the Register, then clear it. It will remain cleared until the monitoring cycle updates it, so the next read operation should not be performed on the register until this has happened, or the result will be invalid. The time taken for a complete monitoring cycle is mainly dependent on the time taken to measure the fan speeds, as described earlier.

The INT output is cleared with the INT_Clear bit, which is Bit 3 of the Configuration Register, without affecting the contents of the Interrupt (INT) Status Registers. When this bit is high, the ADM9240 monitoring loop will stop. It will resume when the bit is low.

TEMPERATURE INTERRUPT MODES

As mentioned earlier, two limit values can be programmed for the temperature measurement, a Hot Temperature Limit (T_{HOT}), and a Hot Temperature Hysteresis Limit ($T_{HOTHYST}$), which is normally some degrees lower.

The interrupt function of the temperature sensor differs from the interrupt operation of the other inputs in that there are three interrupt modes, called "One-Time Interrupt" mode, "Default Interrupt" mode, and "Comparator" Mode.

DEFAULT INTERRUPT MODE

Exceeding T_{HOT} causes an Interrupt that will remain active indefinitely until reset by reading Interrupt Status Register 1 or cleared by the INT_Clear bit in the Configuration register. Once an Interrupt event has occurred by crossing T_{HOT}, then reset, an Interrupt will occur again once the next temperature conversion has completed. The interrupts will continue to occur in this manner until the temperature goes below $T_{HOTHYST}$. Operation in the default interrupt mode is illustrated in figure 10. For clar-

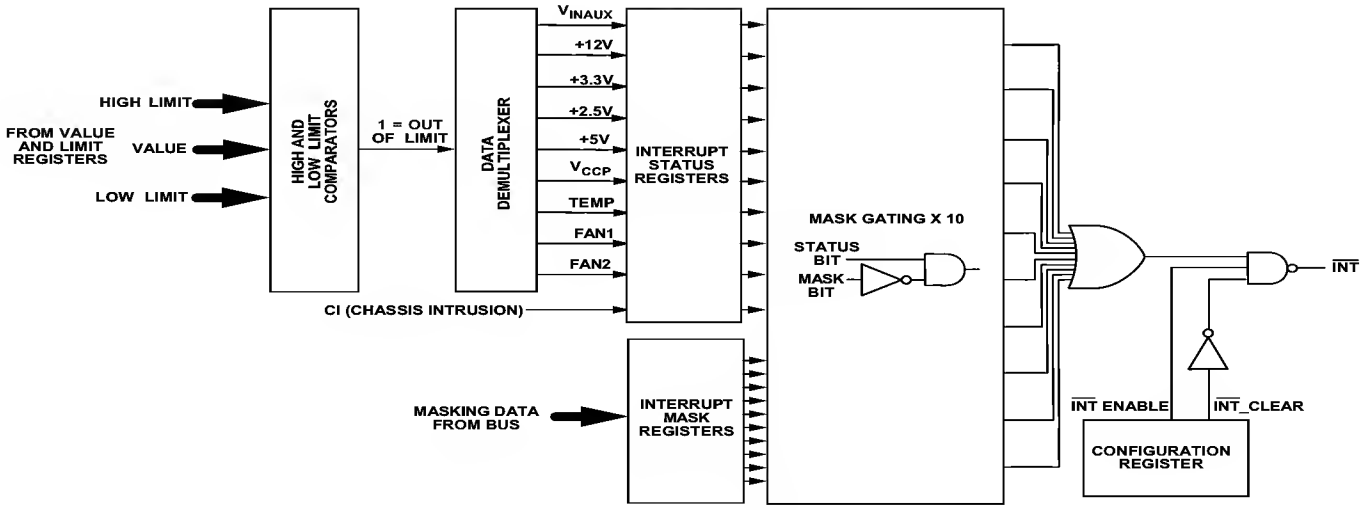


Figure 9. ADM9240 Interrupt Register Structure

ity, in this illustration the interval between read operations is shown as considerably longer than the monitoring cycle time, so that the interrupt is always re-asserted after being reset, before the next read operation occurs.

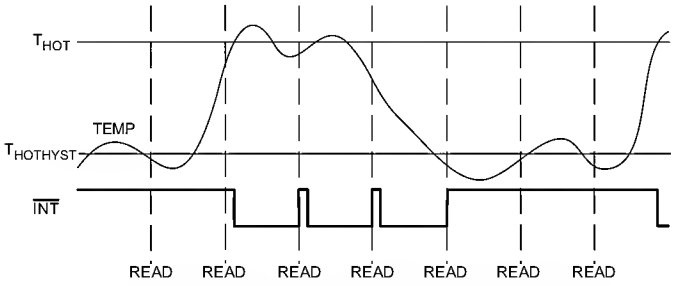


Figure 10. Temperature INT Output in Default Interrupt Mode

ONE-TIME INTERRUPT MODE

Exceeding T_{HOT} causes an Interrupt that will remain active indefinitely until reset by reading Interrupt Status Register 1 or cleared by the INT_Clear bit in the Configuration register. Once an Interrupt event has occurred by crossing T_{HOT}, then reset, an Interrupt will not occur again until the temperature goes below $T_{HOTHYST}$. Operation in the one-time interrupt mode is illustrated in Figure 10. Again, the interval between read operations is shown as being longer than the monitoring cycle time.

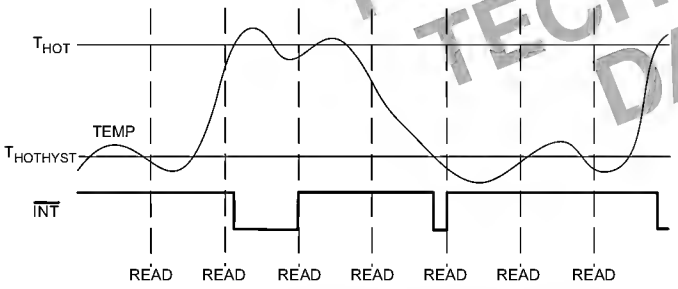


Figure 11. INT Output in One-Time Interrupt Mode

COMPARATOR MODE

Exceeding T_{HOT} causes the INT output to go Low (default). INT will remain Low until the temperature goes below T_{HOT}. Once the temperature goes below T_{HOT}, INT will go High. $T_{HOTHYST}$ is ignored. In other words, Comparator Mode operates like a thermostat with no hysteresis. Operation in the comparator mode is illustrated in Figure 12.

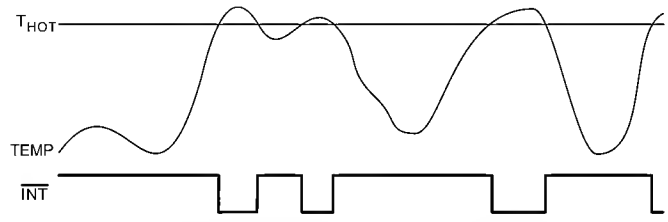


Figure 12. INT Output in Comparator Mode

RESET INPUT/OUTPUT

RESET (pin 12) is an I/O pin that can function as an open-drain output, providing a low-going 20ms output pulse when bit 4 of the Configuration Register is set to 1, provided the reset function has first been enabled by setting bit 7 of Interrupt Mask register 2 to 1. The bit is cleared automatically when the reset pulse is output. Pin 11 can also function as a RESET input by pulling this pin low to reset the internal registers of the ADM9240 to default values. Only those registers that have power on default values as listed in Table 6 are affected by this function. Value and Limit Registers are not affected.

NAND TREE TESTS

A NAND tree is provided in the ADM9240 for Automated Test Equipment (ATE) board level connectivity testing. The device is placed into NAND Test Mode by powering up with pin 11 held high. This pin is sampled automatically after power-up and if it connected high, then the NAND test mode is invoked.

In NAND test mode, all digital inputs may be tested as illustrated below. A0/NTEST_OUT will become the NAND tree output pin. To perform a NAND tree test all pins included in the NAND tree should be driven high.

The structure of the NAND tree is shown in figure 13.

Beginning with A1 and working clockwise around the chip, each pin can be toggled and a resulting toggle can be observed on NTEST_OUT/A0.

Allow for a typical propagation delay of 500 ns.

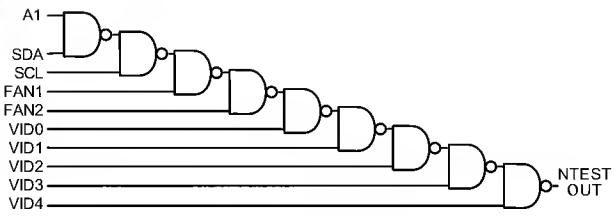


Figure 13. NAND Tree

Note: If any of the inputs shown in figure 9 are unused, they should not be connected direct to ground, but via a low-value resistor such as 10kΩ. This will allow the ATE (Automatic Test Equipment) to drive every input high so that the NAND tree test can be properly carried out.

USING THE ADM9240

POWER ON RESET

When power is first applied, the ADM9240 performs a "power on reset" on several of its registers. Registers whose power on values are not shown have power on conditions that are indeterminate (this includes the Value and Limit Registers). The ADC is inactive. In most applications, usually the first action after power on would be to write limits into the Limit Registers.

Power on reset clears or initialize the following registers (the initialized values are shown in Table 6 on page 18):

- Configuration Register
- Interrupt (INT) Status Register 1
- Interrupt (INT) Status Register 2
- Interrupt (INT) Mask Register 1
- Interrupt (INT) Mask Register 2
- Temperature Configuration Register
- Test Register
- Analog Output Register

INITIALIZATION

Configuration Register INITIALIZATION performs a similar, but not identical, function to power on reset. The Test Register and Analog Output register are not intialized. by this procedure.

Configuration Register INITIALIZATION is accomplished by setting Bit 7 of the Configuration Register high. This Bit automatically clears after being set.

USING THE CONFIGURATION REGISTER

Control of the ADM9240 is provided through the configuration register. The ADC is stopped upon power up, and the INT_Clear signal is asserted, clearing the INT output. The Configuration Register is used to start and stop the ADM9240; enable or disable interrupt outputs and modes, and provides the initialization function described above.

Bit 0 of the Configuration Register controls the monitoring loop of the ADM9240. Setting Bit 0 low stops the monitoring loop and puts the ADM9240 into a low power mode thereby reducing power consumption. Serial bus communication is still possible with any register in the ADM9240 while in low-power mode. Setting Bit 0 high starts the monitoring loop.

Bit 1 of the Configuration Register enables or disables the INT Interrupt output. Setting Bit 1 high enables the INT# output, setting bit 1 low disables the output.

Bit 3 of the Configuration Register is used to clear the INT interrupt output when set high. The ADM9240 monitoring function will stop until bit 3 is set low. Interrupt Status register contents will not be affected.

Bit 4 of the Configuration Register is used to initiate a minimum 20 ms RESET signal on the RESET output if the pin is configured for the RESET mode.

Bit 6 of the Configuration Register is used to reset the Chassis Intrusion (CI) output pin when set high.

Bit 7 of the Configuration Register is used to start a Configuration Register Initialization when taken high.

STARTING CONVERSION

The monitoring function (Analog inputs, temperature, and fan speeds) in the ADM9240 is started by writing to the Configuration Register and setting Start (Bit 0), high, INT_Enable (Bit 1) high, and INT_Clear (Bit 3), low. Apart from initially starting together, the analog mesuerments and fan speed measurements proceed indpendently, and are not synchronised in any way.

The analog measurements will be completed in no more than 353µs (or 5.65ms in averaging mode). The time taken to complete the fan speed measurements depends on the fan speed and the number of tacho output pulses per revolution.

Once the measurements have been completed, their results can be read from the Value Registers at any time.

Table 4 shows the measurement sequence for the analog inputs.

TABLE 4. MEASUREMENT SEQUENCE

MEASUREMENT #	PARAMETER
1	Analog $+V_{CCP2}$
2	Analog $+12V_{IN}$
3	Analog $+5V_{IN}$
4	Analog $+3.3V_{IN}$
5	Analog $+2.5V_{IN}$
6	Analog $+V_{CCP1}$
7	Temperature Reading

SHUTDOWN MODE

The ADM9240 can be placed in a low-power full shutdown mode by setting bit 6 of the Configuration Register to one. This turns off the analog output and stops the monitoring cycle, if running, but it does not affect the condition of any of the registers. The device will return to its previous state when this bit is reset to zero.

APPLICATION CIRCUIT

Figure 14 overleaf shows a generic application circuit using the AD9240. The analog inputs are connected to the power suplies and processor core voltage, VID inputs are connected to the processor Voltage ID pins. There are two inputs from fans, and the analog output is controlling the speed of a third fan. A chassis intrusion latch with an opto-sensor is connected to the CI input. Of course, in an actual application, every input and output may not be used, in which case unused analog and digital inputs should be tied to analog or digital ground as appropriate.

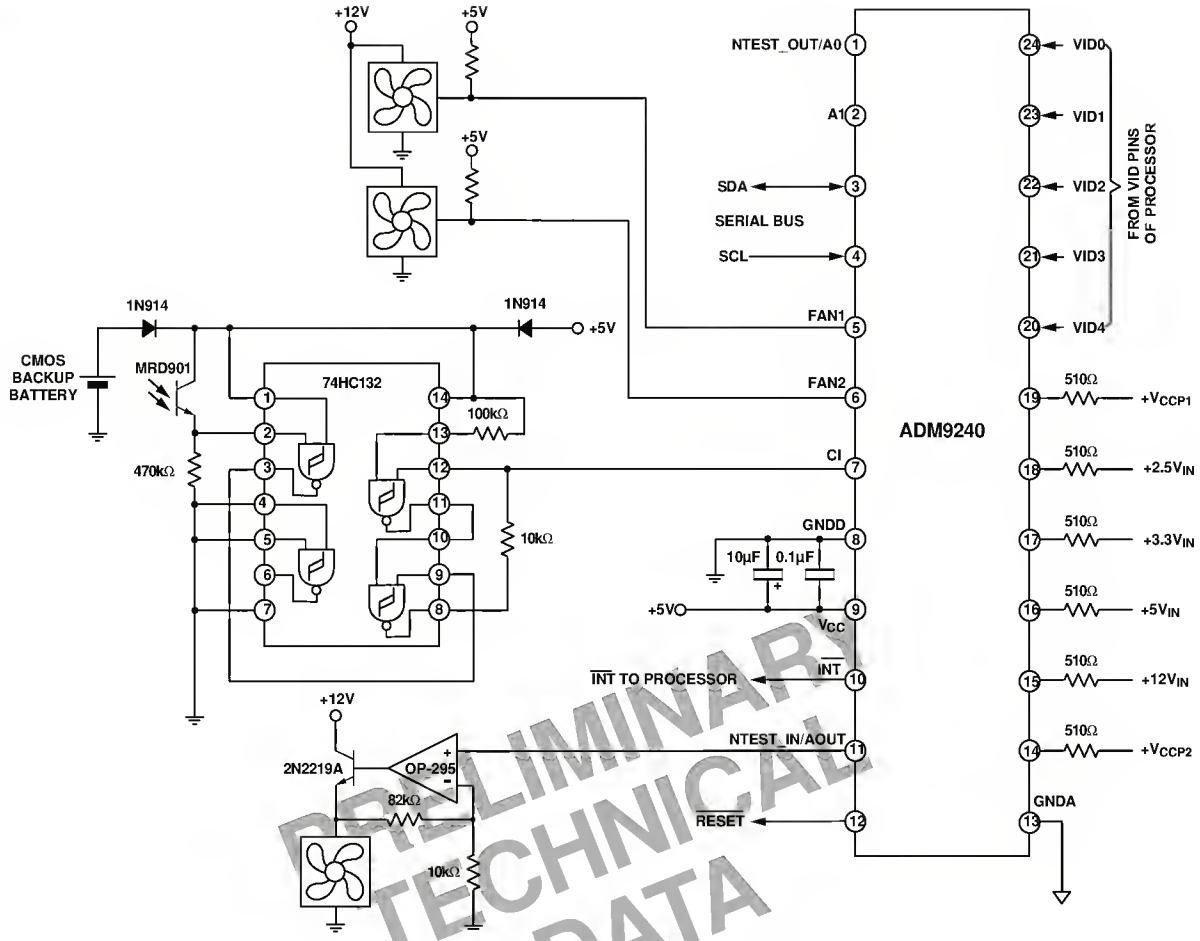


Figure 14. ADM9240 Application Circuit

ADM9240 REGISTERS

TABLE 5. ADDRESS POINTER REGISTER

Bit	Name	R/W	Description
7-0	Address Pointer	Write	Address of ADM9240 Registers. See the tables below for detail.

Address Pointer (Power on default 00h):

TABLE 6. LIST OF REGISTERS

Address A7-A0	Description	Power on Value (Binary Bit 7 - 0)	Notes
15h	Test Register	0000 0000	Setting Bit 0 of this register to 1 selects shutdown mode. Setting bit 7 of this register to 1 selects average measurement mode
19h	Programmed Value of Analog Output	1111 1111	
20h	+2.5V Measured Value	Indeterminate	Read Only
21h	$+V_{CCP1}$ Measured Value	Indeterminate	Read Only
22h	+3.3V Measured Value	Indeterminate	Read Only
23h	+5V Measured Value	Indeterminate	Read Only
24h	+12V Measured Value	Indeterminate	Read Only
25h	V_{CCP2} Measured Value	Indeterminate	Read Only
26h	Reserved	Indeterminate	
27h	Temperature Reading	Indeterminate	Read Only
28h	FAN1 Reading	Indeterminate	Read Only
29h	FAN2 Reading	Indeterminate	Read Only
2Ah	Reserved	Indeterminate	
2Bh	+2.5V High Limit	Indeterminate	
2Ch	+2.5V Low Limit	Indeterminate	
2Dh	$+V_{CCP1}$ High Limit	Indeterminate	
2Eh	$+V_{CCP1}$ Low Limit	Indeterminate	
2Fh	+3.3V High Limit	Indeterminate	
30h	+3.3V Low Limit	Indeterminate	
31h	+5V High Limit	Indeterminate	
32h	+5V Low Limit	Indeterminate	
33h	+12V High Limit	Indeterminate	
34h	+12V Low Limit	Indeterminate	
35h	V_{CCP2} High Limit	Indeterminate	
36h	V_{CCP2} Low Limit	Indeterminate	
37h	Reserved	Indeterminate	
38h	Reserved	Indeterminate	
39h	Hot Temperature Limit (High)	Indeterminate	

TABLE 6. LIST OF REGISTERS (CONTINUED)

Hex	Description Address	Power on Value	Notes (Binary Bit 7 - 0)
3Ah	Hot Temperature Hysteresis Limit (Low)	Indeterminate	
3Bh	FAN1 Fan Count Limit	Indeterminate	
3Ch	FAN2 Fan Count Limit	Indeterminate	
3Dh	Reserved	Indeterminate	
3Eh	Company ID number	0010 0011	This location will contain the company identification number which will be used by software to determine analog voltage curves. This register is read only.
3Fh	Revision number	See Note	This location will contain the revision number of the part. This register is read only.
40h	Configuration Register	0000 1000	See Table 7
41h	Interrupt $\overline{INT}$ Status Register 1	0000 0000	See Table 8
42h	Interrupt $\overline{INT}$ Status Register 2	0000 0000	See Table 9
43h	$\overline{INT}$ Mask Register 1	0000 0000	See Table 10
44h	$\overline{INT}$ Mask Register 2	0000 0000	See Table 11
45h	Compatibility Register		For backwards compatibility.
46h	Chassis Intrusion Clear Register	0000 0000	
47h	VID 0-3/Fan Divisor Register	See note	<7:4> = 0101, <3:0> = VID3 - VID0
48h	Serial Address Register	010 11(A1)(A0)	See Table 15
49h	VID 4 Register	<0>=VID 4	See Table 16
4Bh	Temperature Configuration Register	0000 0001	See Table 17

TABLE 7. REGISTER 40H, CONFIGURATION REGISTER (POWER ON DEFAULT = 08H)

Bit	Name	R/W	Description
0	START	R/W	Logic 1 enables startup of ADM9240, logic 0 places it in standby mode. Caution: The outputs of the Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred (see "INT# Clear" bit). At startup, limit checking functions and scanning begins. Note, all HIGH and LOW LIMITS should be set into the ADM9240 prior to turning on this bit. (Powerup default=0)
1	$\overline{INT}$ Enable	R/W	Logic 1 enables the $\overline{INT}$output. 1=Enabled 0=Disabled (Powerup Default = 0)
2	Reserved		
3	INT_Clear	R/W	During Interrupt Service Routine (ISR) this bit asserted logic 1 clears INT output without affecting the contents of the Interrupt Status Register. The device will stop monitoring. It will resume upon clearing of this bit. (Powerup default=1)
4	RESET	R/W	Creates a RESET (Active Low) signal for 20 ms. minimum (Powerup default = 0) This bit is cleared once the pulse goes active.
5	Reserved	R/W	Default = 0
6	CI_Reset	R/W	Logic 1 resets the chassis intrusion pin. (Powerup default = 0)
7	Initialization	R/W	Logic 1 restores powerup default values to the Configuration register, Interrupt status registers, Interrupt Mask Registers, Fan Divisor Register, and the Temperature Configura tion Register. This bit automatically clears itself since the power on default is zero.

TABLE 8. REGISTER 41H, INTERRUPT STATUS REGISTER 1 (POWER ON DEFAULT = 00 H)

BIT	Name	R/W	Description
0	+2.5V_Error	Read Only	A one indicates a High or Low limit has been exceeded
1	V_{CCP}_Error	Read Only	A one indicates a High or Low limit has been exceeded
2	+3.3V_Error	Read Only	A one indicates a High or Low limit has been exceeded
3	+5V_Error	Read Only	A one indicates a High or Low limit has been exceeded
4	Temp_Error	Read Only	A one indicates that a High or a Low Hot Temperature limit has been exceeded.
5	Reserved	Read Only	Undefined
6	FAN1_Error	Read Only	A one indicates that a fan count limit has been exceeded.
7	FAN2_Error	Read Only	A one indicates that a fan count limit has been exceeded.

TABLE 9. REGISTER 42H, INTERRUPT STATUS REGISTER 2 (POWER ON DEFAULT= 00H)

BIT	Name	R/W	Description
0	+12V_Error	Read Only	A one indicates a High or Low limit has been exceeded
1	V_{CCP2}_Error	Read Only	A one indicates a High or Low limit has been exceeded
2	Reserved	Read Only	Undefined
3	Reserved	Read Only	Undefined
4	Chassis_Error	Read Only	A one indicates Chassis Intrusion has gone high.
5	Reserved	Read Only	Undefined
6	Reserved	Read Only	Undefined
7	Reserved	Read Only	Undefined

Note: Anytime the STATUS Register is read out, the conditions (i.e. Register) that are read are automatically RESET. In the case of the VOLTAGE priority indication, if two or more Voltages were out of LIMITS, then another indication would automatically be generated if it was not handled during the ISR.

In the Control Register, the errant voltage may be disabled, until the operator has time to clear the errant condition or set the limit higher/lower.

TABLE 10. REGISTER 43H, $\overline{INT}$ INTERRUPT MASK REGISTER 1 (POWER ON DEFAULT = 00H)

BIT	Name	R/W	Description
0	+2.5v	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
1	$+V_{CCP1}$	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
2	+3.3v	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
3	+5v	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
4	Temp	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
5	Reserved	Read/Write	Power on default = 0
6	FAN1	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
7	FAN2	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.

TABLE 11.REGISTER 44H, INT MASK REGISTER 2 (POWER ON DEFAULT= 00H)

Bit	Name	R/W	Description
0	+12v	Read/Write	A one disables the corresponding interrupt status bit for INT interrupt.
1	V_{CCP2}	Read/Write	A one disables the corresponding interrupt status bit for INT interrupt.
2	Reserved	Read/Write	Power up default set to Low.
3	Reserved	Read/Write	Power up default set to Low.
4	CI	Read/Write	A one disables the corresponding interrupt status bit for INT interrupt.
5	Reserved	Read/Write	Undefined
6	Reserved	Read/Write	Undefined
7	$\overline{\text{RESET}}$ Enable	Read/Write	A one enables the $\overline{\text{RESET}}$ function in the configuration register

TABLE 12. REGISTER 45H, RESERVED (POWER ON DEFAULT = 00H)

Bit	Name	R/W	Description
0-7	Reserved	Read/Write	Undefined

TABLE 13. REGISTER 46H, CHASSIS INTRUSION CLEAR (POWER ON DEFAULT = 00H)

Bit	Name	R/W	Description
0-6	Reserved	Read/Write	Undefined (Power On = 00h)
7	Chassis Int. Clear.	Read/Write	A one outputs a minimum 20 ms active low pulse on the Chassis Intrusion pin. The register bit clears itself after the pulse has been output.

TABLE 14. REGISTER 47H, VID0-3/FAN DIVISOR REGISTER (POWER ON DEFAULT 0101(VID 3-0))

Bit	Name	R/W	Description
0-3	VID	Read	The VID[3:0] inputs from processor core power supplies to indicate the operating voltage (e.g. 1.3V to 3.5V)
4-5	FAN1 Divisor	Read/Write	Sets counter prescaler for fan speed measurement <3:2> = 00 - divide by 1 <3:2> = 01 - divide by 2 <3:2> = 10 - divide by 4 <3:2> = 11 - divide by 8.
6-7	FAN2 Divisor	Read/Write	Sets counter prescaler for fan speed measurement <3:2> = 00 - divide by 1 <3:2> = 01 - divide by 2 <3:2> = 10 - divide by 4 <3:2> = 11 - divide by 8

TABLE 15. REGISTER 48H, SERIAL ADDRESS REGISTER (POWER ON DEFAULT = 01011(A1)(A0))

Bit	Name	R/W	Description
0-6	Serial Bus Address	Read/Write	SerialBus Address (bit 7 not used)

TABLE 16. REGISTER 49H, VID 4 / DEVICE ID REGISTER (POWER ON DEFAULT 1000000(VID4))

Bit	Name	R/W	Description
0	VID 4	Read	VID 4 Input
1-7	Reserved	Read/Write	

TABLE 17. REGISTER 4BH, TEMPERATURE RESOLUTION REGISTER (POWER ON DEFAULT= 01H)

Bit	Name	Read/Write	Description
0	Hot Temperature Interrupt mode select Bit 0	Read/Write	If Bits 0 and Bits 1 of this register are both zero or one, this selects the default interrupt mode which gives the user an interrupt if the temperature goes above the hot limit. The interrupt will be cleared once the status register is read, but it will again be generated when the next conversion has completed. It will continue to do so until the temperature goes below the ***hysteresis*** limit. A zero on Bit 1 and a one on Bit 0 selects the one time interrupt mode which gives the user an indefinite interrupt when it goes above the hot limit.The interrupt will be cleared once the status register is read. Another interrupt will not be generated until the temperature first goes below the ***hysteresis*** limit. It will also be cleared if the status register is read. No more interrupts will be generated until the temperature goes above the hot limit again. The corre sponding bit will be cleared in the status register every time it is read but may not set again when the next conversion is done.
1	Hot Temperature Interrupt mode select Bit 1	Read/Write	A one on this bit (Bit 1) and a zero on Bit 0 selects the comparator mode. This gives an SMI when the temperature exceeds the hot limit. This SMI remains active until the temperature goes below the ***hot limit (no hys teresis)***, when the SMI will become inactive.
2-6	Reserved	Read/Write	Default = 00000
7	Temp [0]	Read only	LSB of temperature reading = 0.5°C.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Pin TSSOP Package (RU-24)